

## CLAIMS

What is claimed is:

1. A method for basic input output system loading for a personal computer, the method comprising:

    prior to the availability of system memory, storing data in a cache memory disposed in a central processing unit; and

    executing a memory initialization and sizing operation using the data in the cache memory.

2. The method of claim 1 wherein the start-up operation includes a power on self test operation.

3. The method of claim 1 wherein the cache memory is a level one cache.

4. The method of claim 1 wherein the cache memory is a level two cache.

5. The method of claim 1 wherein the start-up operation includes a memory sizing operation.

6. The method of claim 1 wherein the step of passing control of the cache memory includes:

    flushing the cache memory; and

    re-initialize the cache memory.

7. The method of claim 1 wherein the start-up operation is performed by a graphics processor operably coupled to the central processing unit.

8. The method of claim 7 wherein the graphics processor is disposed within a chipset.

9. An apparatus for basic input output system loading, the apparatus comprising:

a graphics processor having a start-up operation.

a central processing unit having a cache memory; and

the graphics processor writing data to the cache memory prior to the start-up operations.

10. The apparatus of claim 9 wherein the start-up operation performed by the graphics processor includes a power on self test operation.

11. The apparatus of claim 9 wherein the start-up operation performed by the graphics processor includes a memory sizing operation.

12. The apparatus of claim 9 wherein the cache memory is a level one cache.

13. The apparatus of claim 9 wherein the cache memory is a level two cache.

14. The apparatus of claim 9 wherein the graphics processor flushes the data from the cache memory and the central processing unit re-initializes the cache memory.

15. The apparatus of claim 14 wherein the central processing unit thereupon utilizes the cache memory.

16. The apparatus of claim 15 wherein the graphics processor is disposed within a chipset.

17. A method for basic input output system loading in a graphics processor, the method comprising:

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prior to the execution of an operating system, storing data in a cache memory disposed in a central processing unit;

establishing a stack assignment within the cache memory;

executing a plurality of executable instructions using the cache memory; and

upon execution of the executable instructions:

flushing the cache memory; and

re-initialize the cache memory; and

passing control of the cache memory to the operating system.

18. The method of claim 17 wherein the executable instructions include a power on self test operation.

19. The method of claim 18 wherein the executable instruction are performed by a graphics processing unit.

20. The method of claim 19 wherein the cache memory is at least one of: a level one cache and a level two cache.